

# JESD204B PHY Layer Compliance Test

By Maury Wood, Scott Ferguson, and Joe Evangelista

Agilent and NXP will provide guidance to design engineers intending to implement 10 Gbps - 12.5 Gbps JESD204B lanes.

## 1.0 Introduction

In the second half of 2012, the first high speed data converters with 10 Gbps JESD204B serial interfaces will be introduced to the market. 10 Gbps per differential lane

is nearly twice the bandwidth of the legacy LVDS DDR parallel interface that JESD204B makes obsolete. Digital radio transceiver design engineers have been quick to adopt this new SerDes-based digital interface, as the cost saving, the technical merits, and the ease-of-use value proposition is compelling. JESD204A lanes run up to 3.125 Gbps, which is relatively easy to implement in conventional PCB materials across 20 cm traces. JESD204B is defined with a maximum of 12.5 Gbps, which requires careful attention to PCB materials, design methods, and PHY layer compliance testing. In this paper, Agilent and NXP will provide guidance to design engineers intending to implement 10 Gbps - 12.5 Gbps JESD204B lanes, and will provide practical advice with respect to maximizing the TX (transmitter) eye opening at the RX (receiver) device. The potential need for TX pre-emphasis and RX equalization will be covered, as will newly proposed PHY layer complaint Method of Implementation (MOI) tests.

## 2.0 JEDEC JESD204B Interface Introduction

The JEDEC standards organization has published three versions of the JESD204 high-speed serial digital interface specification for data converters and logic devices. The first revision, the JESD204 2006 specification, brought the advantag-

es of SerDes-based high-speed serial (3.125 Gbps maximum) interfaces to data converters. The second revision, the JESD204A 2008 specification, added critically important enhancements: the support for multiple data lanes and the support for lane synchronization. Lane synchronization enables JESD204A to be used in quadrature (I/Q) sampling systems, the technology which underpins modern 3G, 3G+ and 4G broadband wireless communications; see Figure 1. A third revision of the specification, JESD204B, has been recently completed by an international JEDEC JC-16 task group (Project 150.01), comprising about 65 members from 25 companies (systems OEMs and semiconductor companies). JEDEC published the JESD204B specification in August 2011. JESD204B introduces three new enhancements that promise to drive this new interface into ubiquitous adoption by data acquisition system engineers worldwide. These enhancements are: a higher maximum lane rate (higher bandwidth); support for deterministic latency through the interface; and support for harmonic frame clocking (or single clock architecture data converters); see Table 1.

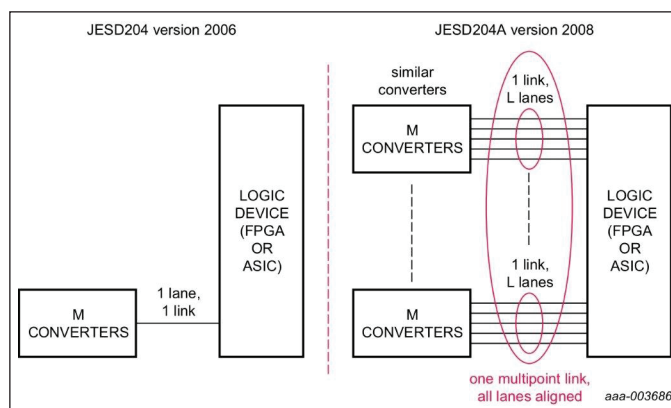


Figure 1 • Lane synchronization enables JESD204A to be used in quadrature (I/Q) sampling systems.

## Layer Compliance Test

There are numerous system design benefits associated with JESD204A/B compared to legacy parallel interfaces. Briefly, these benefits include:

- **Significant** decrease in the number of higher-bandwidth interconnect PCB traces - enabling increased system reliability systems (most failures occur at points of interconnect)
- **Reduced PCB complexity** - impacts both NRE costs and marginal production costs, very often the system can be implemented using fewer PCB layers
- **Opening of a critical bottleneck** in the digital signal processing bandwidth of the system design - enables higher system performance

## 2.1 Deterministic latency - three new device subclasses in JESD204B

In the context of JESD204B, deterministic latency is measured from the parallel frame-based data input of a TX device (typically an ADC), to the parallel frame-based data output of an RX device (typically a DAC), measured within the frame clock domain. JESD204B latency is defined (and is programmable) in units of frame clock cycles or periods. The latency must be precisely repeatable from power-up cycle to power-up cycle, and across link resynchronization events. JESD204B defines three normative Device Subclasses with respect to Deterministic Latency/Harmonic Clocking (DLHC):

- **Device Subclass 0** - has no support for deterministic latency.
- **Device Subclass 1** - defines a new source-synchronous “SYSREF signaling” high-resolution timing (deterministic up to approximately 2 GHz sampling clock frequencies) DLHC protocol, with either a periodic SYSREF, a one-shot (strobe-type) SYSREF or a “gapped periodic” SYSREF distributed to all ADCs/DACs and ASIC/FPGA logic devices. The SYSREF signal synchronizes system-wide local TX and RX frame and multi-frame counters/dividers and the reading of RX FIFO output buffers in JESD204B.
- **Device Subclass 2** - uses the legacy SYNC~ signal, but in a system-synchronous “SYNC~ sampling” low-resolution timing DLHC protocol. This provides accurate deterministic latency up to approximately

	JESD204	JESD204A	JESD204B
JEDEC Specification Release	2006	2008	2011
Maximum Lane Rate (Gbps)	3.125	3.125	12.5
Support for Multiple Lanes	no	yes	yes
Support for Lane Synchronization	no	yes	yes
Support for Multi-Device Synchronization	no	yes	yes
Support for Deterministic Latency	no	no	yes
Support for Harmonic Clocking	no	no	yes

Table 1 • JESD204 specification evolution

500 MHz sampling frequencies, utilizing SYNC~ deassertion to phase adjust ADC, DAC and logic device frame clock and multi-frame clock counters/dividers (combined with control interface-based triggering). The SYNC~ signal conveys interface latency timing information in JESD204B, from the receiver back to the transmitter.

## JESD204B defines new physical clock signals:

- **Device Clock** - a global master clock signal synthesized by a system clock generator circuit from which all TX and RX devices (data converters and logic devices) generate their internal frame clock, and multi-frame clock signals. The device clock period is the absolute timing reference in a JESD204B system. Note that the device clock signal can be a harmonic multiple of the frame clock; this relates directly to the harmonic clocking feature of JESD204B.
- **SYSREF** - a global timing reference signal that can be periodic, one-shot (strobe type), or gapped periodic and used to align frame clock and Local Multi-Frame Clock (LMFC) boundaries. SYSREF is an active HIGH signal that is sampled by the rising edge of the device clock. SYSREF is only used in device subclass 1 systems. The SYSREF source must be the same as the device clock source, typically a crystal oscillator time base, such as a low jitter TCXO or VCO/PLL.

It is helpful to restate the definition of frame, multi-frame and LMFC from the JEDEC JESD204A specification:

- **Frame** - a set of consecutive octets in which the position of each octet can be identified by reference to a frame alignment signal.
- **Multi-frame** - a set of consecutive frames in which the position of each frame can be identified by reference to a multi-frame alignment signal.

- **LMFC** - Local Multi-Frame Clock.

## 2.2 Harmonic frame clocking simplifies the PCB-level clock synthesis and distribution challenge

Simply put, harmonic clocking allows the use of, for example, a 2x, 3x, 4x, 5x, 6x, 7x or 8x sampling frequency (Fs) device clock as the only PCB-level data converter clock, without the need for an additional sampling frequency-based frame clock. The recovered clock from the JESD204B differential input data lane signals is used as the data interface “bit clock”. With harmonic clocking, or single clock system architecture, TX and RX devices can generate all internal clocks from a single clock source, provided that the single clock source is a harmonic multiple of the frame clock.

As a practical example, in the case of a high-speed interpolating DAC architecture, assuming an internal PLL is not used, it is typically required to generate a high-quality device clock signal that is 2x, 4x or 8x the input data rate sampling frequency. This same 2x, 4x, or 8x clock can then be used as the device clock for the ADC, where it is internally divided to create the sampling clock and frame clock.

The advantages of single clock system architectures include reduced IC package pin count and lower risk of detrimental clock feed-through (or crosstalk) effects. In general, fewer clocks at the system PCB level reduce the potential for the disturbance of the ADC and DAC analog performance. At the system PCB level, the design engineer has only one data conversion clock to synthesize and distribute.

## 3.0 Introduction to the OIF-CEI-02.0 specifications

The JESD204A 2008 specification defines an electrical or physical layer (PHY) that supports unidirectional, point-to-point, serial coded data rates from 312.5 Mbps to 3.125 Gbps between data converters and a logic device (FPGA, ASIC, microprocessor or DSP) separated by up to 20 cm of standard FR-4 (FR402/4000-2 and FR406/4000-6) printed-circuit board material. The data converters and logic devices may be connected across a backplane using one or more impedance-controlled connectors or one or more cables.

The JESD204A PHY specification is similar to the OIF (Optical Internetworking Forum) SxI-5 and TFI-5 implementation agreements, generally referred to commercially as Current Mode Logic (CML). Compliant transmitters (TX) and receivers (RX) are expected to achieve Bit Error Rates (BER) of less than  $1E-12$  (see Ref. 1 and Ref. 2).

The JESD204B draft specification additionally defines the OIF Common Electrical Interface (CEI) LV-6G-SR (Short Reach) as the 6.25 Gbps PHY (from 312.5 Mbps to 6.375 Gbps), and the OIF CEI-11G-SR as the 12.5 Gbps PHY. Note that LV-6G-SR compliant transmitters and

receivers are expected to achieve BER of less than  $1E-15$  (see Ref. 5).

Typically, TX pre-emphasis and RX equalization (EQ) on the converters and FPGAs/ASICs is an option at 12.5 Gbps, depending on the length of the transmission line. JESD204B retains the 20 cm “reach” (length) plus one or more impedance-controlled (100 ohm differential) connector transmission line characteristics as JESD204A. High-quality PCB material such as FR-4 Nelco 4000-13SI is also potentially necessary at 12.5 Gbps, again depending on the reach of the transmission line (transmission lines are called data “lanes” in JESD204A/B). Lanes less than 20 cm in length may not require TX pre-emphasis and RX EQ. Like JESD204A, 8B/10B is the coding scheme for JESD204B. Generally speaking, more efficient coders, such as 64B/65B, are used at higher line frequencies, however, it was considered “out of scope” to redefine the coding scheme for JESD204B by the JEDEC 150.01 task group. If there is sufficient industry interest, the coding scheme could be redefined as part of a future JESD204C revision.

The JESD204B specification includes new channel models for the 12.5 Gbps PHY specified as frequency-dependent Insertion Loss Deviation (ILD) masks required for 20 cm FR-4 (FR402/4000-2 and FR406/4000-6) and one or more impedance-controlled connectors or cables. Note that JESD204A specifies insertion loss more simply: the total insertion loss shall not exceed 6 dB from DC to 0.75 times the utilized baud rate.

JESD204A specifies TX and RX return loss (both single-ended and differential) with a single number: 7.5 dB minimum for TX, and 10 dB minimum for RX. In the JESD204B specification, the transmitter differential output return loss minimum (from 100 MHz to 0.75 times the utilized baud rate) is 8 dB, and the common mode return loss minimum (from 100 MHz to 0.75 times the utilized baud rate) is 6 dB. The receiver return loss minimums are the same.

JESD204A defines Total Jitter (TJ) as the sum of Deterministic Jitter (DJ) plus Random Jitter (RJ), measured in peak-to-peak normalized bit times or Unit Intervals (UI). In JESD204A with the 3.125 Gbps PHY, transmitter TJ = 0.35 (p-p) UI, DJ = 0.17 (p-p) UI and RJ = 0.08 (p-p) UI, where UI ranges from 3200 p/s to 320 p/s. The receiver TJ = 0.56 (p-p) UI, DJ = 0.32 (p-p) UI and RJ = 0.24 (p-p) UI over the same range of UI.

In the JESD204B specification, total jitter is defined the same way for 3.125 Gbps and lower speeds. However the transmit jitter budgets for 6 Gbps and up to 12.5 Gbps are defined with limits on TJ, Duty Cycle Distortion (DCD) and Uncorrelated Bounded High Probability Jitter (UBHPJ). UBHPJ is defined as the jitter distribution where the value of the jitter shows no correlation to any signal level being transmitted. The UBHPJ term relates to the traditional Dual Dirac jitter separation model and

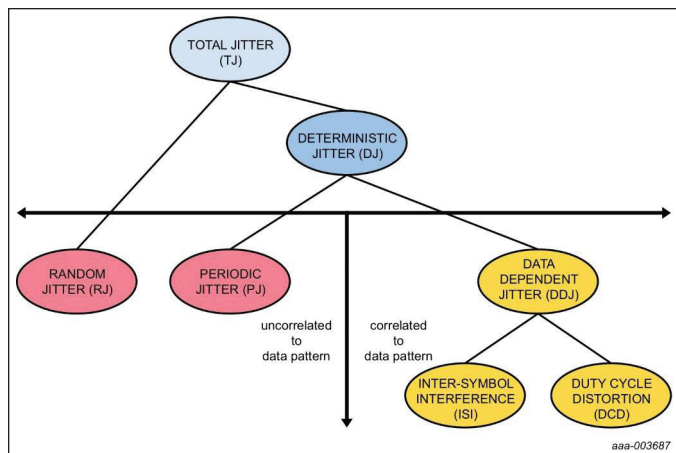


Figure 2 • Jitter.

it is equivalent to the Periodic Jitter (PJ) term shown in Figure 2.

## 4.0 Compliance testing

### 4.1 Tools required for compliance testing

The main tools required for compliance testing of a JESD204B system are:

- Transmitter tests (rise/fall time, jitter, voltage levels) - real-time or sampling oscilloscope.
- Receiver tests (jitter tolerance) - Bit Error Rate Tester (BERT).
- Channel and TX/RX return loss - vector network analyzer or TDR.
- Short circuit current tests - DC supply or source measure unit.

The channel, return loss, and short circuit current measurements are straightforward. The next sections will concentrate on transmitter (TX) and receiver (RX) requirements which bear some consideration.

### 4.2 JESD204B transmitter compliance testing

The transmitter specification for each speed class of JESD204B includes:

- Common mode voltage
- Differential peak-to-peak voltage
- Transmitter short circuit current
- Differential impedance
- Differential output return loss
- Common mode return loss
- Eye mask/jitter

The key requirement for specifying the oscilloscope is the bandwidth. The commonly accepted formula for oscilloscope bandwidth requirements (see Ref. 4) is:

$$BW = 0.4 / (80\% - 20\% \text{ rise time}) \quad (1)$$

where 80 and 20 are percentage of the peak-to-peak voltage levels of the signal. The minimum 80-20 rise time

specified in the LV-OIF-11G-SR operation mode is 24 ps, thereby defining the minimum oscilloscope bandwidth required as 16.7 GHz. Another rule of thumb is to ensure the oscilloscope can measure the 3rd or even 5th harmonic of the signal's fundamental frequency. A 12.5 Gbps data rate has a fundamental frequency of 6.25 GHz. The 3rd harmonic of this data signal is 18.75 GHz, and the 5th harmonic is 31.25 GHz.

Using the rise time rule shows a much lower scope bandwidth rule than the 3rd or 5th harmonic rules. If the signal rise time is limited to at least 24 ps, the higher harmonics are simply not present in the signal. However where the user chooses to probe the signal will determine the harmonic content of the signal. Probing very close to the transmitter will yield more high frequency content than probing at the far end of a PCB channel. So an oscilloscope bandwidth requirement anywhere from 16 GHz to 32 GHz is appropriate for TX testing.

JESD204B specifies that compliant transmitters and receivers are expected to achieve a bit error rate of less than  $1e-12$  for the SxI-5 speed, and less than  $1e-15$  for the 6G-SR and 11G-SR physical layers. Even at the highest speed of 12.5 Gbps, a single loop of  $1e15$  bits would take over 22 hours. So it is impractical to make eye mask and receiver BER measurements to the full bit error rate. Therefore extrapolation is expected. Jitter measurements using the Dual Dirac method on oscilloscopes can easily extrapolate measurements to the targeted BER, assuming adequate measurement data is collected for extrapolation.

The transmitter specifications for 6G-SR and 11G-SR are a combination of eye mask and jitter budget. The jitter budget for the 11G-SR is comprised of:

- Maximum Total Jitter of 0.3 UI (unit interval or bit time)
- Of that 0.3, no more than half (0.15 UI) should be Uncorrelated Bounded High Probability Jitter
- Of the 0.3 TJ limit, no more than 0.05 UI should come from Duty Cycle Distortion (DCD)

There are two terms that are extremely similar with very important differences in their meaning:

- Bounded Uncorrelated Jitter, known and pronounced as "BUJ", is a way of measuring the effects of things like crosstalk in a system.
- Uncorrelated Bounded High Probability Jitter (UBHPJ). UBHPJ is also commonly known as Periodic Jitter, or PJ. PJ is measured as a "delta to delta" value, or the distance between two delta functions that are fit into the jitter histogram (see Ref. 6).

Since all of the transmitter specifications other than return loss and short circuit current can be measured using a real-time scope, a single automation framework can be used to achieve compliance test in the shortest

time with maximum repeatability and minimum risk of operator error.

### 4.3 JESD204B receiver compliance testing

Unlike many other serial digital standards, JESD204B is geared at devices that are inherently unidirectional. Whereas a PCI Express device has both TX and RX in a tightly integrated pair, there is no reason for an ADC to have a JESD204B receiver, or for a DAC to have a JESD204B transmitter. Therefore the traditional BERT methods used for receiver jitter can be difficult to implement. The designer of a JESD204B receiver device must make a choice:

- Implement a bit error rate counter inside the DUT
- Implement a high-speed serial transmitter to be used solely for loopback BER testing

Depending on the choice of receiver test pattern, the implementation of a built-in error counter could be large (and expensive in terms of chip real estate). However the implementation of a true loopback transmitter may be more expensive than a built-in error detector.

The JESD204B specification requires that receiver devices shall be tested using the JTSPAT pattern from INCITS TR-35-2004 (see Ref. 5). This pattern is 1184 bits in length, and an error detector must be capable of achieving bit and frame lock on the pattern, and make a count of bit errors received, and total bits received.

If a DUT is allowed to contain its own bit error rate measurement system, a dilemma arises. The DUT is responsible for declaring its own compliance with the standard (asking the proverbial fox to guard the hen-house). The device should be tested in two ways:

- Transmit the receiver test pattern with specified amount of jitter to simulate the worst case eye as defined in the receiver eye mask; a bit error rate of  $1e-12$  or less is deemed to be passing.
- Transmit the receiver test pattern with minimal jitter, and deliberately inject incorrect bits at a specified rate, and verify that the DUT's error counter measures the same bit error rate being sent into it.

When the DUT's error detector is shown to measure the correct bit error rate with no incoming signal jitter, then it can be trusted to report an accurate measurement on the signal with no transmitted errors but high jitter.

Another key consideration in the design of an on-chip error detector is the ability to query the bit and error counts without disrupting the error rate measurement. If it takes a long period of time to collect results, a user will benefit from knowing if the measurement is going poorly without waiting until the end of the measurement period. Hardware BERT's have been built to provide periodic updates on BER measurements without pausing or disrupting the measurement.

The other challenge to receiver compliance testing is the lack of a specified control interface to the DUT. Many chip vendors will use a standard interface like SPI to

control the chip, but no standardized control protocol has been included as part of the specification. Therefore it is impossible to have a single comprehensive receiver test tool provided by an objective third party. This lack of independently verified methodology creates the risk of interoperability problems due to different receiver test implementations.

If the JC-16 committee determines there is sufficient call to generate a revision of the JESD204B spec, the following items could be considered:

- Specification of a standard control interface like SPI.
- Definition of a standard set of register addresses for setting up on-chip BER measurements (selecting the expected data pattern, starting / stopping tests, querying results during and after completion of a test, checking for bit lock and pattern sync).
- Specification of requirements such as the ability to query BER test results during test execution without disruption of the error rate measurement.

Another possible way to have an external test tool counting the bit error rate would be to use the SYNC~ signal as an indirect method of loopback. In this situation, the receiving device would check for bit errors, and assert the SYNC~ output signal whenever a received bit does not match the expected bit in the pattern. The SYNC~ output could then be connected to a BERT error



**Figure 3 • Receiver equalization techniques such as DFE and CTLE allow the receiver to improve the eye opening.**

detector. The BERT would expect to see a pattern of all zeros, and anytime a one is received it would increment the bit error count. This would require that the SYNC~ output signal be capable of running at the full data rate of the data lanes.

A compliant receiver is expected to achieve a bit error rate of less than  $1e-15$ . Recognizing this is impractical to directly measure, JESD204B allows that the test can apply adjustments to the Gaussian Jitter portion of the receive eye masks and measure only to a BER of  $1e-12$ .

A test signal matching the receiver test eye mask contains a “cocktail” of various types of jitter including Random Jitter, Periodic or Sinusoidal Jitter, and ISI. In many cases it is impractical to directly generate ISI so many pulse generators provide a signal with a mixture of random and periodic jitter, and then employ external physical channels (referred to as “Golden Channels”) to

apply ISI to the test signal. This method will require calibration with an oscilloscope (see Ref. 7).

Another consideration on the use of eye masks for receiver tests at speeds up to 12.5 Gbps is the fact that there will typically be no eye opening at all at the receiver. Channel losses from lengthy traces of PCB materials will completely collapse the eye. Transmitter de-emphasis can help make up for channel loss, but not enough at high speeds. Receiver equalization techniques such as DFE and CTLE (see Figure 3.) allow the receiver to improve the eye opening as well (see Ref. 8). It is impractical to probe the signal after the equalizer and before the receiver. Equalization modeling packages are available on oscilloscopes so that simulated receiver equalization can be applied to a signal that is probed close to the RX. While JESD204B doesn’t explicitly describe this method, an assumption could be made that the jitter profile on the BERT pulse generator should be set up such that the receive eye mask is met after applying receiver equalization.

#### 4.4 Approaching a Method of Implementation (MOI) for compliance testing

There are many different requirements for compliance testing of JESD204B. Running each measurement by hand can be very time consuming, and also introduces the risk of variability in results due to operator errors or misinterpretations of instructions. Therefore an ideal MOI would automate the entire suite of measurement requirements. Because of the nature of JESD204B this is not entirely possible, but steps can be taken to strive for the best possible implementation. For example:

- All transmitter tests can be automated into a single software program that controls an oscilloscope.
- Receiver stressed eye calibration can be achieved using automated scope tools similar to Seasim used in PCI Express 3.0.

An MOI for JESD204B compliance testing will essentially be an application note describing how to achieve

each of the spec measurements. It will be accompanied by a set of software tools, instrument configuration files to enable accurate and repeatable results, and to maximize the probability of interoperability between compliant devices.

#### 4.5 Conclusions

The commercial availability of JESD204B compliant receivers (specifically high speed DACs) has brought the technical challenges of RX PHY layer test into sharp focus. These challenges become more daunting as the data lane frequency approaches the specification limit of 12.5 Gbps.

It is clear that the inclusion of specific, standardized test registers (both control and status, typically accessed through an SPI interface on high speed converters) with specified functionality would make PHY layer compliance testing much easier for the end (OEM) customer. The JEDEC JC-16 Project 150.01 Task Group which developed the JESD204B specification should consider including the “control interface” within the scope of JESD204, should there be industry interest in moving forward with a JESD204C revision.

The authors also recommend that JESD204C specify control and status registers on the TX device and the RX device to facilitate “logical” (transport and data link layer) compliance and interoperability testing. Other specification enhancements which might be within scope

of JESD204C include an increase in maximum lane frequency above 12.5 Gbps, potentially on links shorter than the currently specified 20 cm, and potentially on an impedance-controlled substrate with TX pre-emphasis and RX equalization.

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